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REMARKS/ARGUMENTS

The Office Action of January 31, 2008, has been carefully reviewed and these remarks are responsive thereto. Claims 1-25 remain pending in this application. No changes have been made to the claims. The listing of claims is provided for the examiner's convenience. Reconsideration and allowance of the instant application are respectfully requested.

Summary of Telephonic Examiner Interview

Applicants thank examiner Ghandi for the telephonic interview with Applicant's in-house counsel, Tom Evans, and Applicant's undersigned representative, on March 11, 2008. This section, along with the remainder of this paper, provides the requisite interview summary required by 37 C.F.R. § 1.133.

During the interview, Applicants discussed the following:

- **Issue 1**: The failure of the Office Action to make a prima facie rejection of claim 1. Specifically, the Office Action of January 31, 2008, fails to address all the limitations of claim 1. See first full paragraph on page 3 of the Office Action for details. One example of a deficiency is the failure of the Office Action to identify where the Herron reference teaches or suggests "configuring a configurable logic block of the first set as a verifier to verify a responsive output of the second set organized into *M* groups of configurable logic blocks, wherein the verifier is configured to accept its own output as one bit of the *N*-bit input, wherein, upon the output of the verifier being a failure indicator, the verifier is configured to maintain the failure indicator for the test" as claimed. **Outcome**: agreement was reached that the Heron reference is deficient, and also that the Office Action does not establish a prima facie rejection of claims 1-6, 10, and 12.
- **Issue 2**: Applicants argued that the Flanagan reference is inapplicable as applied in the following rejections:

> 7. Claims 13, 14, 15, 16, 17, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Butts et al. (US 5,036,473) in view of Cote et al. (US 6,470,485 B1) and Flanagan et al. (US 6,141,334).

and

10. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng et al. (US 5,903,744) in view of Butts et al. (US 5,036,473), Cote et al. (US 6,470,485 B1) and Flanagan et al. (US 6,141,334).

Specifically, Flanagan describes CDMA wireless telecommunications, and has no application to creation and testing of a logic circuit. **Outcome**: Agreement was reached that the Flanagan reference is inapplicable, and the Office Action thus fails to establish a prima facie rejection of 13-17, 23, and 25.

- **Issue 3**: Patentability of claims 18 and 24. **Outcome**: Applicants agreed to submit arguments and/or amendments with their next filing (see below).

Rejections Under 35 U.S.C. § 103

Claims 1, 2, 3, 4, 5, 6, 10 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 6,760,277, hereinafter Farooq, in view of U.S. Pat. No. 6,996,758, hereinafter Herron et al. Applicants traverse, based on the arguments presented above, for which agreement has already been reached with the Office. It is therefore Applicant's understanding and belief that the Office will either allow or issue a non-final rejection of claims 1-6, 10, and 12 in a subsequent paper.

Claims 7 and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Farooq and Herron et al. as applied to claim 6 above and further in view of U.S. Pat. No. 6,621,767, hereinafter Kattan. Applicants traverse insofar as Kattan does not cure the aforementioned deficiencies of Herron, and claims 7 and 8 are therefore allowable for at least the same reasons as their respective base claims. Applicants reserve the right to address the merits of the Kattan reference at a future time as needed.

Claims 13, 14, 15, 16, 17 and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 5,036,473, hereinafter Butts et al., in view of U.S. Pat. No. 6,470,485, hereinafter Cote et al. and U.S. Pat. No. 6,141,334, hereinafter Flanagan et al. Claim 25 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tseng et al, in view of Butts et al, Cote et al. and Flanagan et al. Applicants traverse, based on the arguments presented above, for which agreement has already been reached with the Office. It is therefore Applicant's

understanding and belief that the Office will either allow or issue a non-final rejection of claims 13-17, 23, and 25 in a subsequent paper.

Claims 18-20 and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Cote et al., in view of U.S. Pat. No. 6,874,107, hereinafter Lesea. Applicants respectfully traverse.

Even if combined, Cote and Lesea do not teach or suggest all the features of independent claim 18. For example, claim 18 recites, *inter alia*, "a data processing portion coupled to the first set, the data processing portion configured to provide a first test pattern to the first set, wherein the first set is configured to provide a second test pattern to test the second set." The Office Action alleges that such a feature is described in Cote. Cote, however, at the cited locations or elsewhere, does not teach or suggest such a feature.

For example, at the cited portion of col. 1, lines 10-13, Cote states:

> The invention relates generally to integrated circuits having repeated configurable logic and configurable interconnect structures provided therein. The invention relates more specifically to the problem of thoroughly and quickly testing large numbers and different types of interconnect resources such as those provided within an integrated circuit monolith that contains a programmable logic circuit such as a field programmable gate array (FPGA).

There is no recitation above regarding a data processing portion configured to provide a first test pattern to the first set, wherein the first set is configured to provide a second test pattern to test the second set, as claimed. Instead, Cote describes the general nature of the invention with providing specific details of its workings.

At the cited portion of col. 17, line 66-col. 18, line 3, Cote states:

> length' (10×RL) VGB-interconnecting lines 308.
> Although not fully shown in FIG. 3A, a 'VGB', as the term is used herein, is a Variable Grain Block structure
>
> **18**
>
> which, in one set of embodiments, includes at least four user-programmable LUT's such as 4-LUT's **350–380** and at least eight associated registers such as **355***a*–**385***b*. Sectional line **390** indicates the boundaries for one such VGB in FIG. 3A. See also FIG. 3B which shows a plurality of VGB's **390***a*, **390***b* and **390***c* within the surrounding environments of their respective L-OSM and G-OSM.

There is also no recitation above regarding a data processing portion configured to provide a first test pattern to the first set, wherein the first set is configured to provide a second

test pattern to test the second set, as claimed. Instead, Cote describes the makeup of Variable Grain Block structure as including lookup tables (LUTs) and associated registers.

At the cited portion of col. 23, lines 48-50, Cote states:

> ISM's **330** and **340**. A given first VGB can be programmed to produce signals that are output onto one of the global clock lines **303** of the integrated circuit device. The excita-

There is also no recitation above regarding a data processing portion configured to provide a first test pattern to the first set, wherein the first set is configured to provide a second test pattern to test the second set, as claimed. Instead, Cote describes conventional outputting of signals onto a global clock line.

At the cited portion of col. 24, lines 1-17, Cote states:

> Referring again to FIG. **3B**, an alternate method for obtaining faster read-out of pass/fail test results is shown. Substantially identical sequential state machines, **300***a* and **300***c* are implemented respectively by VGB-A (**390***a*), VGB-C (**390***c*), and their respective interconnect resources. Cross-exchange of state feedback signals is optionally permissible as indicated by dashed lines **393**. This cross-exchange can be used for testing the full continuity of a 2×RL lines such as the one shown inside VIC **391**. An excitational test signal can be injected from SwBk-A (**320***a*) into one terminal end of the illustrated vertical 2×RL line while the line-propagated result is acquired by SwBk-C (**320***c*) from the opposed terminal end and fed into a verification point within VGB-C (**390***c*). If the vertical 2×RL line is broken or stuck low or stuck high, sequencer **300***c* should responsively be thrown off its expected phase and the defect should thereby be detected. It is not a good idea to use

There is also no recitation above regarding a data processing portion configured to provide a first test pattern to the first set, wherein the first set is configured to provide a second test pattern to test the second set, as claimed. Instead, Cote describes cross-exchange of feedback signals for testing the continuity of 2xRL lines.

At the cited portion of col. 25, lines 6-26, Cote states:

> FIG. 3C shows yet another implementation in accordance with the invention. The feedback loop of an FPGA-implemented sequencer need not comprise just one VGB and its adjacent interconnect resources. A loop can be composed of plural VGB's and can use one or more of the registers in each VGB for storing current state bits. Although FIG. 3C shows just VGB-A and VGB-M positioned within a feedback loop with their respective register sets inline with the loop, it is within the contemplation of the invention to use more such combinations of decoder-implementing LUT's and registers in each loop and/or to activate the register-bypass mechanisms, **399***a* or **399***m*, of a subset of these LUT's as may be useful for testing the register-bypass mechanisms (**399***a*, **399***m*) and/or for creating different excitational patterns in various segments of each of the testing loops. If VGB-A and VGB-M are widely spaced apart (e.g., 10, 20 or more rows/columns apart) they may be used to test in one FPGA configuration, the end-to-end continuities of 10×RL lines. Synchronized clockings of the respective register sets of each LUT-implemented decoder may be provided by way of the global clock wires in the FPGA.

There is also no recitation above regarding a data processing portion configured to provide a first test pattern to the first set, wherein the first set is configured to provide a second test pattern to test the second set, as claimed. Instead, Cote describes a feedback loop of an FPGA-implemented sequencer.

At the cited portion of col. 25, lines 33-47, Cote states:

> FIG. 4A illustrates a perspective view of a computerized testing system **400** that may be programmably configured to operate in accordance with the invention. This view may be used to reiterate some of the basic discussions provided above about testing a stream of FPGA dies or of packaged chips in a mass production environment. Illustrated FPGA device **401** is one of a mass production stream of like-manufactured devices that are provided either as part of an exposed set of dies on wafers that are being tested in a final wafer-sort facility or as packaged IC devices that are being tested in a post-packaging test facility. Prober **402** is correspondingly either a wafer-sort probe head that comes down into contact with an under-test FPGA die (**401**) or a test socket which comes into interfacing contact with an under-test and packaged IC device (**401**). In a mass production

There is also no recitation above regarding a data processing portion configured to provide a first test pattern to the first set, wherein the first set is configured to provide a second test pattern to test the second set, as claimed. Instead, Cote describes a computerized testing workstation.

At the cited portion of col. 26, lines 35-42, Cote states:

> Referring now to FIG. 4B, a possible method for interconnecting components of computer system **400** is shown schematically. Computer system **400** may include a central processing unit (CPU) **450** or other data processing means (e.g., plural processors), and a system memory **460** for storing immediately-executable instructions and immediately-accessible data for the CPU **450** or other processors. System memory **460** typically takes the form of

There is also no recitation above regarding a data processing portion configured to provide a first test pattern to the first set, wherein the first set is configured to provide a second test pattern to test the second set, as claimed. Instead, Cote describes the interconnection of components within the computerized testing workstation.

At the cited portion of col. 27, lines 9-13 and 18-40, Cote states:

> tions in accordance with the present invention. The instructing signals and/or data signals that are transferred through the communications network **490** for causing system **400** to perform said operations may also be manufactured and structured in accordance with the present invention.
>
> System memory **460** may hold executing portions **461** of an operating system (OS) and of any then-executing parts of application programs **465**. The application programs **465** generally communicate with the operating system by way of an *API* (application program interface) **461a**. One of the application programs **465** may be an FPGA configuring and testing program structured to cause the FPGA to self-test itself in accordance with the invention described herein. System memory **460** may include various data structures for causing computer system **400** to perform various operations in accordance with the present invention as described herein.
>
> *Although the embodiment of FIG. 4A is described as* providing a single station **400** for both configuring supplied FPGA's **(401)** for self-testing of themselves and for reading out the self-test results **422** and for comparing **(423)** the read-out results against expected results **(421)**, it is within the contemplation of the invention to carry out such steps serially at two or more stations rather than all in one place. In other words, a first station may simultaneously and in-parallel program a large batch of FPGA's to run a respective first test. A plurality of next stations may individually probe the FPGA die/IC packages **401** and cause them to execute the first test while collected the read-out states at appropriate pause points. A third machine may collect test results, analyze them, and provide test-result reports. A wide variety of modifications are possible to the basic theme.

There is also no recitation above regarding a data processing portion configured to provide a first test pattern to the first set, wherein the first set is configured to provide a second test pattern to test the second set, as claimed. Instead, Cote describes the computerized testing workstation performing certain test functions.

In addition to the above, the Office Action concedes that Cote does not teach or suggest the claimed *N*-bit input generator, or that the first set is configured to provide a configurable logic block, separate from the *N*-bit input generator, as a verifier to verify the output data of the second set, as claimed. Instead the Office Action relised on Lesea col. 2, lines 34-42 and col. 6, lines 54-67. However, having reviewed the cited portions of Lesea and elsewhere in Lesea, Applicants find no relevance to the presently claimed subject matter.

For example, at col. 2, lines 34-42, Lesea states:

> In another embodiment, a field programmable gate array (FPGA) comprises input and output data communication connections, a serializer/deserializer circuit coupled to the input and output data communication connections, and a logic array programmed to generate a test data pattern coupled to the output data connection. The logic array is further programmed to check a data pattern received on the input connection while performing a built in self test operation. After test, the circuit may be re-programmed as stated above.

Lesea does not teach or suggest the claims N-bit input generator nor the verifier, as claimed.

At the cited portion of col. 6, lines 54-67, Lesea states:

> 13. A method of testing a serializer/deserializer (SERDES) circuit of a field programmable gate array (FPGA) comprising:
> programming a logic array of the FPGA;
> generating a test pattern using the programmed logic array of the FPGA;
> outputting the test pattern on an output connection of the SERDES circuit;
> externally coupling the test pattern to an input connection of the SERDES circuit;
> using the programmed logic array, evaluating data received on the input connection;
> storing data indicating a result of the evaluation in a memory circuit of the FPGA; and

Lesea is similarly deficient at this location as well.

Claims 19, 20, and 22 are allowable for at least the same reasons as their respective base claims, and further in view of the additional features recited therein. For example, with respect to claim 22, Cote fails to teach or suggest that an output of the verifier is an input to the verifier, and wherein the output of the verifier is a failure indicator, as claimed. Instead, at the cited location of col. 25, lines 6-26 (reproduced above), Cote describes a general feedback loop, but not the claimed output of the verifier being used as an input to the verifier.

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Claim 24 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 5,903,744, hereinafter Tseng at al., in view of Cote et al. Applicants respectfully traverse.

The Cote reference is deficient with respect to claim 24 at least in similar ways as the Cote reference is deficient with respect to claim 18, discussed above, and Tseng does not cure the aforementioned deficiencies of Cote. Claim 24 is therefore allowable over the art of record.

CONCLUSION

All issues having been addressed, Applicant respectfully submits that the instant application is in condition for allowance, and respectfully solicits prompt notification of the same. However, if for any reason the Examiner believes the application is not in condition for allowance or there are any questions, the Examiner is requested to contact the undersigned at (202) 824-3153.

Respectfully submitted,

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